Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. 1OE**
2. **1A0**
3. **2Y3**
4. **1A1**
5. **2Y2**
6. **1A2**
7. **2Y1**
8. **1A3**
9. **2Y0**
10. **GND (2 bond pads)**
11. **2A0**
12. **1Y3**
13. **2A1**
14. **1Y2**
15. **2A2**
16. **1Y1**
17. **2A3**
18. **1Y0**
19. **N. 2OE**
20. **VCC (2 bond pads)**

**.096”**

**.067”**

**2 1 20**

**3**

**4**

**5**

**6**

**7**

**8**

**9 10 11**

**19**

**18**

**17**

**16**

**15**

**14**

**13**

**12**

**AC244T**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: AC244T**

**APPROVED BY: DK DIE SIZE .067” X .096” DATE: 12/4/17**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54AC240**

**DG 10.1.2**

#### Rev B, 7/1